Application
Note

Kodak KSC-1000 Programming Examples - KAI-11000 Image Sensor

October 4, 2004
Revision 1.0

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TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

INTRODUCTION

The KSC-1000 is a programmable CCD timing generator that is designed to interface with the entire family of Kodak Interline and Full-Frame area array CCDs. The KSC-1000 uses traditional registers for defining the 13 pixel rate clocks, electronic shutter pulse generation, and general setup and control. Line Tables are used to define 6 outputs during the vertical clocking interval. Frame Tables are used to sequence the line table to create an image frame and to control portions of an imaging system. The KSC-1000 can be programmed to control image system timing or be slaved to an external controller.

This application note presents several examples of Line Table and Frame Table programming. The General Setup Register and the INTG-STRT Setup programming examples are also covered.

LINE TABLE EXAMPLES

I/O Mapping

The KSC-1000 line tables are used to define the states of the signals V1, V2, V3, V4, V5, and V6. These signals are used as inputs to a vertical clock driver circuit. It is assumed that a non-inverting driver circuit is used for the examples below. The I/O map for the examples is detailed in Table 1 below.

Note that two KSC-1000 outputs are required to generate the three levels required for the KAI-2020 V2 input. Note that on power up, the KAI-11000 V2 input will be at the V2 low level since the KSC-1000 V2 output defaults to logic 0. This selects the low level of the 3 level driver circuit.

KSC-1000 Output	KAI-0340 Driver	Logic 1 Selection	Logic 0 Selection
V1	V1 Driver	Mid V1 Level	Low V1 Level
V2	V2 (High-Mid)-Low Drive	V2 High-Mid Driver Selection	Low V2 Level
V3	V2 High-Mid Driver	High V2 Level	Mid V2 Level
V4	FD Driver	High Fast Dump Level	Low Fast Dump Level
V5	Not Used		
V6	Not Used		

Table 1 KSC-1000 to KAI-11000 Vertical Clock Driver Signal Map

Figure 1 is a copy of the Frame Timing diagram from the KAI-11000 Device Performance Specification. This diagram shows the vertical clocking required to transfer the charge from all of the photodiodes to the Vertical CCD (VCCD). Vertical clocking for transferring the charge from the VCCD to the Horizontal CCD (HCCD) is also shown.

Frame Timing – Continuous Mode

Frame Timing without Binning

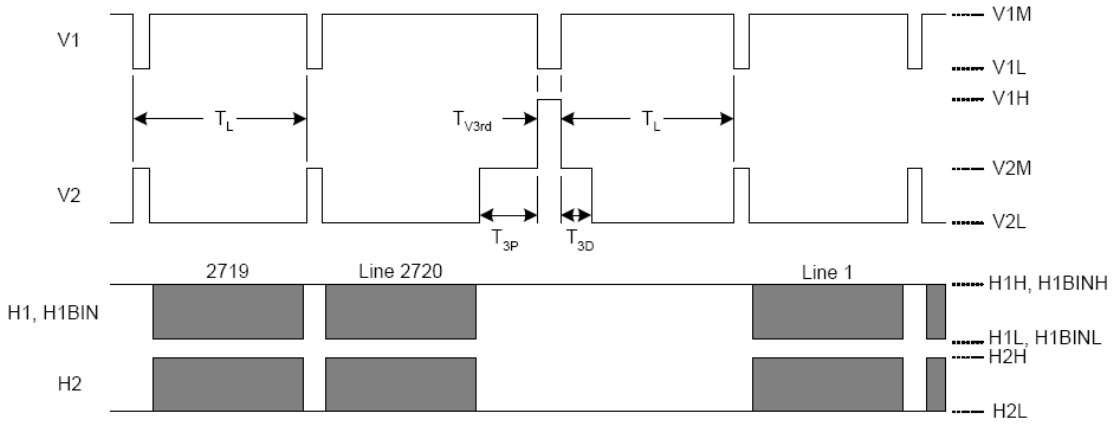

Figure 1 KAI-11000 Frame Timing

Table 2 lists the Timing Requirements for the KAI-11000. The pixel clock period is assumed to be 33nS for the examples that follow. The value in the count field is the number of pixel clock cycles that are required to produce the desired time period. For example, 106 pixel clock periods of 33nS each are required to produce the 3.5uS nominal T_{VCCD} time.

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
HCCD Delay	T_{HD}	3.0	3.5	10.0	µs	
VCCD Transfer time	T_{VCCD}	3.0	3.5	20.0	µs	
Photodiode Transfer time	T_{V3rd}	8.0	10.0	15.0	µs	
VCCD Pedestal time	T_{3P}	100.0	120.0	200.0	µs	
VCCD Delay	T_{3D}	15.0	20.0	80.0	µs	
Reset Pulse time	T_R	2.5	5.0		ns	
Shutter Pulse time	T_S	3.0	4.0	10.0	µs	
Shutter Pulse delay	T_{SD}	1.0	1.5	10.0	µs	
HCCD Clock Period	T_H	33		200	ns	
VCCD rise/fall time	T_{VR}	0.0	0.1	1.0	µs	
Fast Dump Gate delay	T_{FD}	0.5			µs	
Vertical Clock Edge Alignment	T_{VE}	0.0		100	ns	

Table 2 KAI-11000 Timing Requirements

Line Table 0 – Photodiode to VCCD Transfer

Table 3 is an example of a line table that implements the vertical clocking timing shown for Figure 1. This line table covers the period from the beginning of T_{3P} to the end of T_L. The table uses the signal mappings described above. The line table address of 0 is an arbitrary selection. The frame table architecture permits random accessing of the line tables. The pixel clock period is assumed to be 33nS.

Entry	Label	Value	Time	Comment
0	Count	3636	120uS	3636 33nS clock periods required for a 120uS period
0	HCLK_H	0		Set to 0, not last active entry in the line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	0		Fast Dump Driver at low level
0	V3	0		V2 High-Mid driver at mid level
0	V2	1		V2 driver at mid level
0	V1	1		V1 driver at mid level

1	Count	303	10uS	303 33nS clock periods required for a 10uS period
1	HCLK_H	0		Set to 0, not last active entry in the line table
1	V6	0		Not Used
1	V5	0		Not Used
1	V4	0		Fast Dump Driver at low level
1	V3	1		V2 High-Mid driver at high level
1	V2	1		V2 driver at high level
1	V1	0		V1 driver at low level
2	Count	606	20uS	606 33nS clock periods required for a 20uS period
2	HCLK_H	0		Set to 0, not last active entry in the line table
2	V6	0		Not Used
2	V5	0		Not Used
2	V4	0		Fast Dump Driver at low level
2	V3	0		V2 High-Mid driver at mid level
2	V2	1		V2 driver at mid level
2	V1	1		V1 driver at mid level
3	Count	3266	109uS	3266 33nS clock periods required for a 109 uS period
3	HCLK_H	0		Set to 0, do not start horizontal readout after this entry
3	V6	0		Not Used
3	V5	0		Not Used
3	V4	0		Fast Dump Driver at low level
3	V3	0		V2 High-Mid driver at mid level
3	V2	0		V2 driver at low level
3	V1	1		V1 driver at mid level
4	Count	0	0	All zero entry to indicate end of line table
4	HCLK_H	0		
4	V6	0		
4	V5	0		
4	V4	0		
4	V3	0		
4	V2	0		
4	V1	0		

Table 3 Line Table 0 for Photodiode to VCCD Transfer

To program this line table, the user initiates a write to register 9, the Line Table Access Register. The 8-bit line table address is programmed next. The address consists of an entry number followed by the table number. The 5 20 bit data entries complete the bit stream for this register.

The serial data is always written LSB first. The Line Table Address needs to written 1 time only if the auto-incrementing feature of the Line Table serial interface is used. The entries are programmed in ascending order starting at the entry number specified in the Line Table Address. Program execution from a line table always starts at entry 0. The bit streams for Line Table 0 (Table 3 above) are shown in the Table 4 below.

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 0**						
Line Table Address Bit Stream	0000	0000						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	0010110001110	0	0	0	0	0	1	1
Entry 1 Bit Stream	1111010010000	0	0	0	0	1	1	0
Entry 2 Bit Stream	0111101001000	0	0	0	0	0	1	1
Entry 3 Bit Stream	0100001100110	0	0	0	0	0	0	1
Entry 4 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 4 Line Table 0 Bit Stream

Line Table 1 – Single Vertical Clock Cycle

Figure 2 shows the timing required to shift 1 line in the vertical CCD and readout 1 line from the horizontal CCD.

Line Timing Dual Output

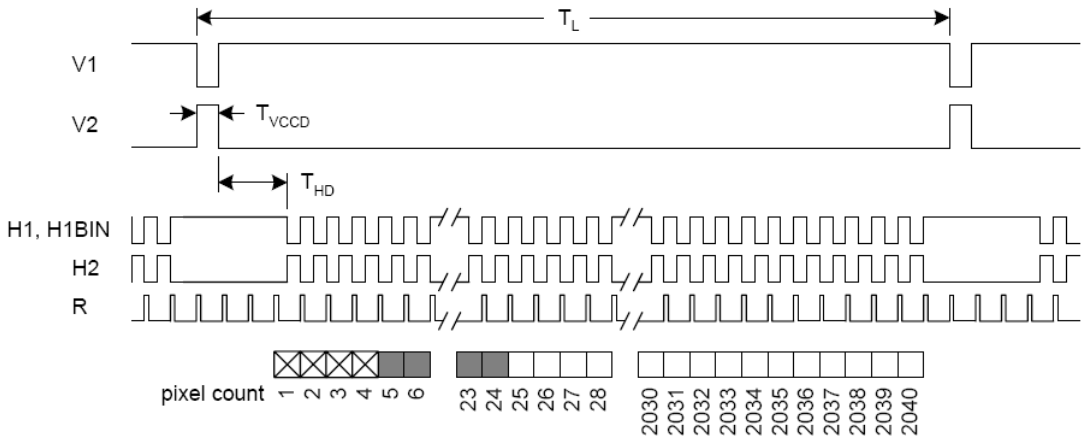

Figure 2 KAI-11000 Line Timing

Table 5 is an example of a line table that shows the vertical clocking sequence shown in Figure 2. This line table is assigned to address 1.

Entry	Label	Value	Time	Comment
0	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS pulse
0	HCLK_H	0		Set to 0, not last active entry in the line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	0		Fast Dump Driver at low level
0	V3	0		V2 High-Mid driver at mid level
0	V2	1		V2 driver at mid level
0	V1	0		V1 driver at low level
1	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS period
1	HCLK_H	1		Set to 1, proceed to horizontal readout upon completion of line table
1	V6	0		Not Used
1	V5	0		Not Used
1	V4	0		Fast Dump Driver at low level
1	V3	0		V2 High-Mid driver at mid level
1	V2	0		V2 driver at low level
1	V1	1		V1 driver at mid level
2	Count	0	0	All zero entry to indicate end of line table
2	HCLK_H	0		
2	V6	0		
2	V5	0		
2	V4	0		
2	V3	0		
2	V2	0		
2	V1	0		

Table 5 Line Table 1 for Vertical CCD Shift and Horizontal CCD Readout.

The serial bit stream for Line Table 1 is shown in Table 6 below:

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 1**						
Line Table Address Bit Stream	0000	1000						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	0101011000000	0	0	0	0	0	1	0
Entry 1 Bit Stream	0101011000000	1	0	0	0	0	0	1
Entry 2 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 6 Line Table 1 Bit Stream

Line Table 2 – Vertical Binning by 2

Figure 3 shows the timing requirements for binning 2 rows in the VCCD.

Line Timing Vertical Binning by 2

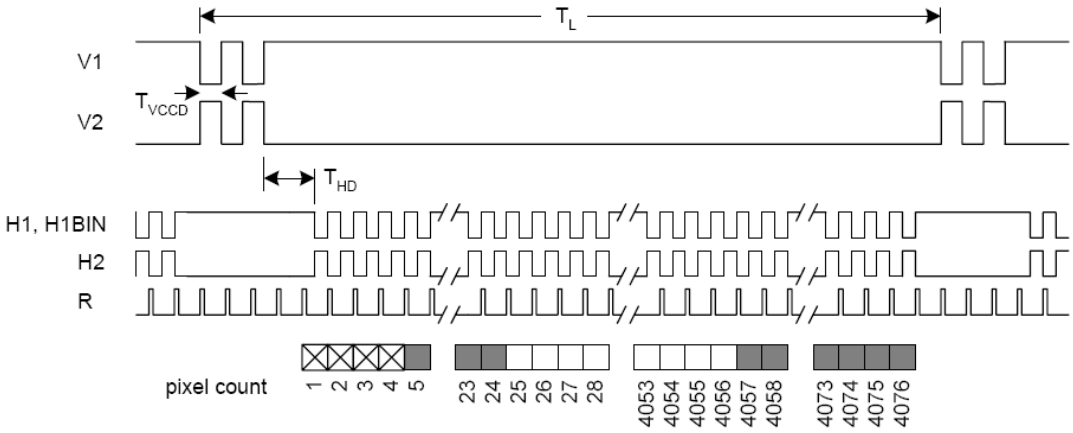

Figure 3 Timing for Vertical Binning by 2.

Table 7 is an example of a line table that implements the vertical binning shown in Figure 3. This line table is assigned to address 2.

Entry	Label	Value	Time	Comment
0	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS pulse
0	HCLK_H	0		Set to 0, not last active entry in the line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	0		Fast Dump Driver at low level
0	V3	0		V2 High-Mid driver at mid level
0	V2	1		V2 driver at mid level
0	V1	0		V1 driver at low level
1	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS pulse
1	HCLK_H	0		Set to 0, not last active entry in the line table
1	V6	0		Not Used
1	V5	0		Not Used
1	V4	0		Fast Dump Driver at low level
1	V3	0		V2 High-Mid driver at mid level
1	V2	0		V2 driver at low level
1	V1	1		V1 driver at mid level
2	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS pulse
2	HCLK_H	0		Set to 0, not last active entry in the line table
2	V6	0		Not Used
2	V5	0		Not Used
2	V4	0		Fast Dump Driver at low level
2	V3	0		V2 High-Mid driver at mid level
2	V2	1		V2 driver at mid level
2	V1	0		V1 driver at low level
3	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS pulse
3	HCLK_H	1		Set to 1, proceed to horizontal readout upon completion of line table
3	V6	0		Not Used
3	V5	0		Not Used
3	V4	0		Fast Dump Driver at low level
3	V3	0		V2 High-Mid driver at mid level
3	V2	0		V2 driver at low level
3	V1	1		V1 driver at mid level

4	Count	0	0	All zero entry to indicate end of line table
4	HCLK_H	0		
4	V6	0		
4	V5	0		
4	V4	0		
4	V3	0		
4	V2	0		
4	V1	0		

Table 7 Line Table 2 Vertical Binning by 2

The serial bit stream for Line Table 2 is shown in Table 8 below

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 2**						
Line Table Address Bit Stream	0000	0100						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	0101011000000	0	0	0	0	0	1	0
Entry 1 Bit Stream	0101011000000	0	0	0	0	0	0	1
Entry 2 Bit Stream	0101011000000	0	0	0	0	0	1	0
Entry 3 Bit Stream	0101011000000	1	0	0	0	0	0	1
Entry 4 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 8 Line Table 2 Serial Bit Stream

Line Table 3 – Fast Dump Timing

Figure 4 shows the timing requirements for fast dumping 3 lines and transferring the 4th line into the VCCD. T_{FD} is set to its nominal value of 0.5uS for this table.

Fast Line Dump Timing

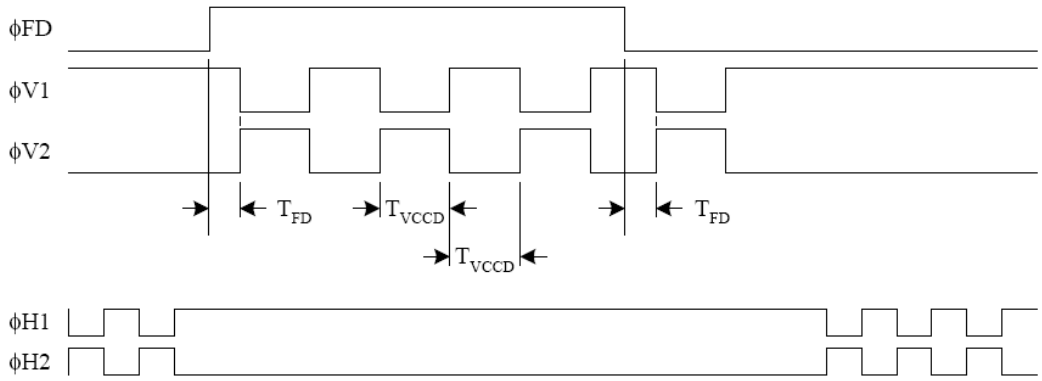

Figure 4 Fast Dump 3 Lines and transfer 4th line to the VCCD.

Table 9 is an example of a line table that shows the vertical clocking sequence shown in Figure 4. This line table is assigned to address 3.

Entry	Label	Value	Time	Comment
0	Count	15	500nS	15 33nS clock periods required for a 500nS period
0	HCLK_H	0		Set to 0, not last active entry in the line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	1		Fast Dump Driver at high level
0	V3	0		V2 High-Mid driver at mid level
0	V2	0		V2 driver at low level
0	V1	1		V1 driver at mid level
1	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS period
1	HCLK_H	0		Set to 0, not last active entry in the line table
1	V6	0		Not Used
1	V5	0		Not Used
1	V4	1		Fast Dump Driver at high level
1	V3	0		V2 High-Mid driver at mid level
1	V2	1		V2 driver at mid level
1	V1	0		V1 driver at low level
2	Count	106	3.5uS	106 33nS clock periods required for a 1.5uS period
2	HCLK_H	0		Set to 0, not last active entry in the line table
2	V6	0		Not Used
2	V5	0		Not Used
2	V4	1		Fast Dump Driver at high level
2	V3	0		V2 High-Mid driver at mid level
2	V2	0		V2 driver at low level
2	V1	1		V1 driver at mid level
3	Count	106	3.5uS	106 25nS clock periods required for a 3.5uS period
3	HCLK_H	0		Set to 0, not last active entry in the line table
3	V6	0		Not Used
3	V5	0		Not Used
3	V4	1		Fast Dump Driver at high level
3	V3	0		V2 High-Mid driver at mid level
3	V2	1		V2 driver at mid level
3	V1	0		V1 driver at low level

4	Count	106	3.5uS	106 25nS clock periods required for a 3.5uS period
4	HCLK_H	0		Set to 0, not last active entry in the line table
4	V6	0		Not Used
4	V5	0		Not Used
4	V4	1		Fast Dump Driver at high level
4	V3	0		V2 High-Mid driver at mid level
4	V2	0		V2 driver at low level
4	V1	1		V1 driver at mid level
5	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS period
5	HCLK_H	0		Set to 0, not last active entry in the line table
5	V6	0		Not Used
5	V5	0		Not Used
5	V4	1		Fast Dump Driver at high level
5	V3	0		V2 High-Mid driver at mid level
5	V2	1		V2 driver at mid level
5	V1	0		V1 driver at low level
6	Count	91	3uS	91 33nS clock periods required for a 3uS period
6	HCLK_H	0		Set to 0, not last active entry in the line table
6	V6	0		Not Used
6	V5	0		Not Used
6	V4	1		Fast Dump Driver at high level
6	V3	0		V2 High-Mid driver at mid level
6	V2	0		V2 driver at low level
6	V1	1		V1 driver at mid level
7	Count	15	500nS	15 33nS clock periods required for a 500nS period
7	HCLK_H	0		Set to 0, not last active entry in the line table
7	V6	0		Not Used
7	V5	0		Not Used
7	V4	0		Fast Dump Driver at low level
7	V3	0		V2 High-Mid driver at mid level
7	V2	0		V2 driver at low level
7	V1	1		V1 driver at mid level

8	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS period
8	HCLK_H	0		Set to 0, not last active entry in the line table
8	V6	0		Not Used
8	V5	0		Not Used
8	V4	0		Fast Dump Driver at low level
8	V3	0		V2 High-Mid driver at mid level
8	V2	1		V2 driver at mid level
8	V1	0		V1 driver at low level
9	Count	106	3.5uS	106 33nS clock periods required for a 3.5uS period
9	HCLK_H	1		Set to 1, proceed to horizontal readout upon completion of line table
9	V6	0		Not Used
9	V5	0		Not Used
9	V4	0		Fast Dump Driver at low level
9	V3	0		V2 High-Mid driver at mid level
9	V2	0		V2 driver at low level
9	V1	1		V1 driver at mid level
10	Count	0	0	All zero entry to indicate end of line table
10	HCLK_H	0		
10	V6	0		
10	V5	0		
10	V4	0		
10	V3	0		
10	V2	0		
10	V1	0		

Table 9 Line Table 3 Fast Dump Clocking

The serial bit stream for Line Table 3 is shown in Table 10 below:

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 3**						
Line Table Address Bit Stream	0000	1100						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	1111000000000	0	0	0	1	0	0	1
Entry 1 Bit Stream	0101011000000	0	0	0	1	0	1	0
Entry 2 Bit Stream	0101011000000	0	0	0	1	0	0	1
Entry 3 Bit Stream	0101011000000	0	0	0	1	0	1	0
Entry 4 Bit Stream	0101011000000	0	0	0	1	0	0	1
Entry 5 Bit Stream	0101011000000	0	0	0	1	0	1	0
Entry 6 Bit Stream	1101101000000	0	0	0	1	0	0	1
Entry 7 Bit Stream	1111000000000	0	0	0	0	0	0	1
Entry 8 Bit Stream	0101011000000	0	0	0	0	0	1	0
Entry 9 Bit Stream	0101011000000	1	0	0	0	0	0	1
Entry 10 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 10 Line Table 3 Serial Bit Stream

Line Table 4 – Idle State

An idle state will be used to allow reprogramming of the General Setup register. This register will need to be reprogrammed when switching between center column readout and full image readout. This line table holds V2 at the V_{2L} level and holds V1 at the V_{1M} level. The horizontal readout state will not entered upon completion of the line table. A period of 142uS, which corresponds to a full image single output readout line time, is arbitrarily chosen. The idle state line table can be called repeatedly until the programming cycle is completed.

Entry	Label	Value	Time	Comment
0	Count	4260	142uS	4260 33nS clock periods required for a 142uS period
0	HCLK_H	0		Set to 0, do not start horizontal readout upon completion of line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	0		Fast Dump Driver at low level
0	V3	0		V2 High-Mid driver at mid level
0	V2	0		V2 driver at low level
0	V1	1		V1 driver at mid level
1	Count	0	0	All zero entry to indicate end of line table
1	HCLK_H	0		
1	V6	0		
1	V5	0		
1	V4	0		
1	V3	0		
1	V2	0		
1	V1	0		

Table 11 Line Table 4 Idle State Timing

The serial bit stream for Line Table 4 is shown in Table 12 below:

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 4**						
Line Table Address Bit Stream	0000	0010						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	0010010100001	0	0	0	0	0	0	1
Entry 1 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 12 Line Table 4 Serial Bit Stream

FRAME TABLE EXAMPLES

Frame Tables are used to link together a sequence of line tables. The following examples switch between Fast Dump Decimated Readout, and Full Image Readout modes. Frame Table 0 is configured for a Fast Dump Decimated Readout sequence. Frame Table 2 is configured for a Single Output Full Image Readout sequence. The VD event is used to switch between image modes.

Frame Table 0

Entry 0 is an example of the ExLT command. This entry calls Line Table 0. That Line Table is used to transfer charge from the photodiodes to the Vertical CCD. This entry also clears the vertical line counter. All clamping is disabled in this entry. Frame Valid, Line Valid, and PBLK are disabled. The vertical line counter is cleared in this entry.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	1	Clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	1	Execute Line Table 0 1X, proceed to next entry when finished
Address 2:0	0	
Address 3	0	

Table 13 Frame Table 0, Entry 0

Entry 1 is another example of the ExLT command. This entry calls Line Table 3. This line table fast dumps 3 lines and transfers a single line to the horizontal CCD. The line table is called 3 times to fast dump a total of 9 dark lines. A total of 3 dark lines are read out, but are not stored as Line Valid and Frame Valid are disabled for this entry. Horizontal readout is enabled after each completion of this line table. The Pixels Per Line field of the General Setup Register is programmed to a value of 2040 assuming dual channel readout is used. The vertical line counter is enabled for this line. The line rate clamps and PBLK are disabled. The frame rate clamps are enabled.

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Disable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	1	Enable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	1	Enable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	3	Execute Line Table 3 3x, proceed to next entry when finished
Address 2:0	3	
Address 3	0	

Table 14 Frame Table 0, Entry 1

Entry 2 implements the ExLT command. This entry calls Line Table 3 three times. This table fast dumps 3 dark lines and reads out the last dark line on the first pass. It also fast dumps a total of 6 active buffer lines and reads out a 2 active buffer lines. The vertical line counter is enabled for this entry. The frame rate clamps are disabled while the line rate clamps are enabled. Frame Valid and Line Valid are disabled. PBLK is disabled.

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Enable Line Valid
Frame Valid Enable	0	Enable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	3	Execute Line Table 3 3x, proceed to next entry when finished
Address 2:0	3	
Address 3	0	

Table 15 Frame Table 0, Entry 2

Entry 3 implements ExLT command again. This entry calls line table 1002 times to fast dump and read out the active video lines. Horizontal readout is enabled after completion of this line table. The vertical line counter is enabled for this entry. Line Valid and Frame Valid are enabled. PBLK is disabled. Frame rate clamping is disabled while line rate clamping is enabled.

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	1	Enable Line Valid
Frame Valid Enable	1	Enable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	1002	Execute Line Table 3 1002x, proceed to next entry when finished
Address 2:0	3	
Address 3		

Table 16 Frame Table 0, Entry 3

Entry 4 implements the ExLT command again. This entry calls line table 3 six more times. Horizontal readout is enabled after completion of this line table. This first execution of this entry fast dumps 3 active buffer lines and 12 dark lines. 1 active buffer line and 4 dark lines are clocked out. The vertical line counter is enabled. Line Valid, Frame Valid, and PBLK are disabled. Frame rate clamping is disabled while line rate clamping is enabled.

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	6	Execute Line Table 3 six times, proceed to next entry when finished
Address 2:0	3	
Address 3	0	

Table 17 Frame Table 0, Entry 4

Entry 5 is an implementation of the JmpFTVD command. If a VD event has been registered, control jumps to Frame Table 1 to enter the Single Channel Full Image Readout mode. Otherwise, operation continues with Entry 6 in this Frame Table. Signals that are activated at programmed pixel counts such as PBLK, line valid, frame valid, frame rate clamps, and line rate clamps are not activated with this command regardless of the state of the control bit. Only the ExLT or the ExLTNVD commands directly execute line tables which in turn can start the horizontal state machine.

Label	Value	Comment
Check and Increment Line Counter	0	Increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	0	Jump to Entry 0 of Frame Table 1 if a VD event has been registered. Continue operation with Entry 6 of Frame Table 0 if no VD event has been registered.
Address 2:0	1	
Address 3	1	

Table 18 Frame Table 0, Entry 5

Entry 6 is an example of the JmpFT command. Control jumps back to entry 0 of this Frame Table. This architecture provides a continuous capture loop. Entry 5 provides an escape from the continuous loop when an external controller provides a VD signal. Signals that are activated at programmed pixel counts such as PBLK, line valid, frame valid, frame rate clamps, and line rate clamps are not activated with this command regardless of the state of the control bit. Only the ExLT or the ExLTNVD commands directly execute line tables which in turn can start the horizontal state machine.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Do not Enable Line Valid
Frame Valid Enable	0	Do not enable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Set PBLK high
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	0	Jump to Entry 0 of Frame Table 0
Address 2:0	0	
Address 3	0	

Table 19 Frame Table 0, Entry 6

To program Frame Table 0, the user initiates a write to register 8, the Frame Table Access Register. The 7-bit frame table address is programmed next. The address consists of an entry number followed by the table number. The 7 34 bit data entries complete the bit stream for this register.

The serial data is always written LSB first. The Frame Table Address needs to written 1 time only if the auto-incrementing feature of the Line Table serial interface is used. The entries are programmed in ascending order starting at the entry number specified in the Line Table Address. Program execution from a frame table always starts at entry 0. The bit streams for Frame Table 0 are shown in the Table 20 below.

Some of the individual control bits have been grouped in the table below. The INTG_STRT Cntl field consists of the Check and Increment Line Counter Bit (LSB), followed by Clear Line Counter Bit and the Force INTG_START bit in that order. The H Bin field consists of 2 bits. The Enables field consists of the HCLK_V Enable bit (LSB) followed by the Line Valid Enable bit, the Frame Valid Enable bit, the Video Amplifier Enable bit, the AFE Clock Enable bit, the CLPDM2 Enable bit, the CLPDM1 Enable bit, the CLPOB2 Enable bit, the CLPOB1 Enable bit, and the PBLK enable bit in that order. The count field contains 13 bits.

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	0	0	0	1			
Line Table Address Label	**Entry 0**	**Addr 0**						
Line Table Address Bit Stream	0000	000						
Data Entry Label	**INTG_STRT Cntl**	**H Bin**	**Enables**	**PBLK Idle**	**Flag**	**Count**	**A0:2**	**A3**
Entry 0 Bit Stream	010	00	0001100000	1	0	1000000000000	000	0
Entry 1 Bit Stream	100	00	0001101010	1	0	1100000000000	110	0
Entry 2 Bit Stream	100	00	0001110100	1	0	1100000000000	110	0
Entry 3 Bit Stream	100	00	0111110100	1	0	0101011111000	110	0
Entry 4 Bit Stream	100	00	0001110100	1	0	0110000000000	110	0
Entry 5 Bit Stream	000	00	0001100000	1	0	0000000000000	100	1
Entry 6 Bit Stream	000	00	0001100000	1	0	0000000000000	000	0

Table 20 Frame Table 0 Serial Bit Stream

Frame Table 1

Frame Table 1 implements the Idle State. Line Table 4 maintains inactive vertical clocks for a period of 142uS. This is the time required to clock out 1 horizontal line in the Single Output Full Image Readout mode. Horizontal Readout is not triggered after completion of the line table. The vertical counter, Frame Rate clamp, Line Rate clamp, Frame Valid, Line Valid, and PBLK are all disabled in Frame Table 1.

Frame Table 1 uses the VD event to control mode switching. Entry 0 uses the ExLTNVD instruction to call Line Table 4 repeatedly until the external controller generates a VD signal. The external controller can use the Idle State to reprogram the General Control Register to set up for the Single Output Full Image Capture mode. Once the VD event is detected, execution of Line Table 4 is completed and program control is passed on to Entry 1.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not Clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	1	
Count	0	Execute Line Table 4 repeatedly until a VD event is detected.
Address 2:0	4	
Address 3	0	

Table 21 Frame Table 1, Entry 0

Entry 1 is an ExLT instruction. The Idle State is called one more time to allow the external controller to generate an additional VD signal if the control is to be passed to Frame Table 2. In the event that no VD signal is generated, control is passed back to Frame Table 0.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not Clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	1	Execute Line Table 4 1x.
Address 2:0	4	
Address 3	0	

Table 22 Frame Table 1, Entry 1

Entry 2 is a JmpFTVD instruction. If a VD signal was detected, control is passed to Frame Table 2 Entry 0 to start the Single Output Full Image Capture mode. Otherwise, entry 3 is executed.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not Clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	0	Jump to Frame Table 2 Entry 0.
Address 2:0	2	
Address 3	1	

Table 23 Frame Table 1, Entry 2

Entry 3 is a JmpFT instruction. Control is passed to Frame Table 0.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not Clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	0	Jump to Frame Table 0 Entry 0.
Address 2:0	0	
Address 3	0	

Table 24 Frame Table 1, Entry 3

The serial bit stream for Frame Table 1 is shown in Table 25 below.

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	0	0	0	1			
Line Table Address Label	**Entry 0**	**Addr 0**						
Line Table Address Bit Stream	0000	100						
Data Entry Label	**INTG_STRT Cntl**	**H Bin**	**Enables**	**PBLK Idle**	**Flag**	**Count**	**A0:2**	**A3**
Entry 0 Bit Stream	000	00	0001100000	1	1	0000000000000	001	0
Entry 1 Bit Stream	000	00	0001100000	1	0	1000000000000	001	0
Entry 2 Bit Stream	000	00	0001100000	1	0	0000000000000	010	1
Entry 3 Bit Stream	000	00	0001100000	1	0	0000000000000	000	0

Table 25 Frame Table 1 Serial Bit Stream

Frame Table 2

Frame Table 2 implements the Single Output Full Image Readout mode. Entry 0 calls Line Table 0 once, utilizing the ExLT command. This entry generates the timing necessary to transfer the charge from the pixels to the vertical CCD. The line counter is cleared with this entry. Frame Valid, Line Valid, frame rate clamping, line rate clamping, and PBLK are disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	1	Clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	1	Execute Line Table 1 once; proceed to next entry when finished.
Address 2:0	0	
Address 3	0	

Table 26 Frame Table 2, Entry 0

Entry 1 utilizes the ExLT command again. Line Table 1 is called 2 times to clock out the first two dark lines. The line counter is activated in this entry. Frame Valid, Line Valid, the frame rate clamps, and PBLK are all disabled. The line rate clamps are enabled.

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	2	Execute Line Table 1 2x; proceed to next entry when finished.
Address 2:0	1	
Address 3	0	

Table 27 Frame Table 2, Entry 1

Entry 2 is another ExLT instruction. Line Table 1 is called 12 times to clock out the next group of 12 dark lines. The vertical line counter is enabled. Frame Valid, Line Valid, and the line rate clamps are disabled. Frame rate clamping is enabled. PBLK is also disabled.

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	1	Enable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	1	Enable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	12	Execute Line Table 1 12x; proceed to next entry when finished.
Address 2:0	1	
Address 3	0	

Table 28 Frame Table 2, Entry 2

Entry 3 implements the ExLT command. This entry calls Line Table 1 10 times to clock out the last 2 top dark lines and all 8 top active buffer lines. The vertical line counter remains enabled. Frame Valid and Line Valid are disabled. Line rate clamping is enabled in this entry. Frame rate clamping along with PBLK are disabled.

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	10	Execute Line Table 1 10x, proceed to next entry when finished
Address 2:0	1	
Address 3	0	

Table 29 Frame Table 2, Entry 3

Entry 4 is implements the ExLT command again. This entry calls Line Table 1 4008 times to clock out all of the active video rows. The vertical line counter is enabled for this entry. The frame rate clamps are disabled and the line rate clamps are enabled. Frame Valid, Line Valid are disabled. PBLK is disabled

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	1	Enable Line Valid
Frame Valid Enable	1	Enable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	4008	Execute Line Table 1 4008x, proceed to next entry when finished
Address 2:0	1	
Address 3	0	

Table 30 Frame Table 2, Entry 4

Entry 5 implements the ExLT command. This entry calls Line Table 1 24 times to clock out the 8 active buffer rows and 16 dark rows on the bottom of the sensor. The vertical line counter is enabled for this entry. The frame rate clamps are disabled while the line rate clamps are enabled. Frame Valid, Line Valid and PBLK are disabled.

Label	Value	Comment
Check and Increment Line Counter	1	Increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	24	Execute Line Table 1 24x, proceed to next entry when finished
Address 2:0	1	
Address 3	0	

Table 31 Frame Table 2, Entry 5

Entry 6 implements the JmpFT command. This entry passes control back to Frame Table 1, which places the imaging system in idle mode.

Label	Value	Comment
Check and Increment Line Counter	0	Increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT		Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable		Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable		Enable AFE Clocks
CLPDM2 Enable	0	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable		Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val		PBLK active low
Flag	0	
Count	0	Jump to entry 0 of Frame Table 1
Address 2:0		
Address 3	0	

Table 32 Frame Table 2, Entry 6

The serial bit stream for programming Frame Table 2 is shown in Table 33 below.

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	0		0	1			
Line Table Address Label	**Entry 0**	**Addr 2**						
Line Table Address Bit Stream		010						
Data Entry Label	**INTG_STRT Cntl**	**H Bin**	**Enables**	**PBLK Idle**	**Flag**	**Count**	**A0:2**	**A3**
Entry 0 Bit Stream	010	00	0001100000	1	0	1000000000000	000	0
Entry 1 Bit Stream	100	00	0001110100	1	0	0100000000000	100	0
Entry 2 Bit Stream	100	00	0001101010	1	0	0011000000000	100	0
Entry 3 Bit Stream	100	00	0001110100	1	0	0101000000000	100	0
Entry 4 Bit Stream	100	00	0111110100	1	0	0001010111110	100	0
Entry 5 Bit Stream	100	00	0001110100	1	0	0001100000000	100	0
Entry 6 Bit Stream	000	00	0001100000	1	0	0000000000000	100	0

Table 33 Frame Table 2 Serial Bit Stream

FLUSH IMPLEMENTATION

The KSC-1000 can easily be programmed to flush the KAI-11000 image sensor. The vertical clock pulse width and the duration between vertical clock pulses are defined in the line table. The HCLK_V Enable bit is set in the frame table entry in which the flush line table is called. This allows the horizontal clocks to run during the vertical interval time. The HCLK_H Enable bit in the line table is not set in the last entry. This prevents the KSC-1000 from entering the horizontal readout state and causes the flush line table to be executed repeatedly until the termination condition for the frame table entry is satisfied. Table 34 below is an example of a fast flush implementation that generates vertical clock pulses every 6uS.

Entry	Label	Value	Time	Comment
0	Count	90		90 33nS clock periods required for 3uS pulse
0	HCLK_H	0		Set to 0, not last active entry in the line table
0	V6	0		FD low
0	V5	0		V2C High-Mid driver at mid level
0	V4	1		V2C driver at mid level
0	V3	0		V2 High-Mid driver at mid level
0	V2	1		V2 driver at mid level
0	V1	0		V1 driver at low level
1	Count	90		90 33nS clock periods required for 3uS period
1	HCLK_H	0		Do not proceed to horizontal readout upon completion of line table
1	V6	0		FD low
1	V5	0		V2C High-Mid driver at mid level
1	V4	0		V2C driver at low level
1	V3	0		V2 High-Mid driver at mid level
1	V2	0		V2 driver at low level
1	V1	1		V1 driver at mid level
2	Count	0		All zero entry to indicate end of line table
2	HCLK_H	0		
2	V6	0		
2	V5	0		
2	V4	0		
2	V3	0		
2	V2	0		
2	V1	0		

Table 34 Fast Flush Line Table

LINE RATE ELECTRONIC SHUTTERING

The Force INTG_STRT bit can be used to implement line rate electronic shuttering. This bit is set for those frame table entries in which line rate electronic shuttering is desired. Since the INTG_STRT timing sequence is executed before the line table, each line in which the Force INTG_STRT bit is set will be lengthened by the duration of the INTG_STRT setup, pulse, and hold times.

EXTENDED INTEGRATION TIME

Integration time can easily be extended beyond the frame readout time. After completion of the frame readout an ExLTNVD instruction can be used to extend the integration time indefinitely. The line table could either park the vertical clocks in their idle state or continue the image frame readout clocking to over-clock the sensor. Horizontal clocks could optionally be disabled to save power. This approach requires the system controller to provide a VD signal to terminate the integration period.

Integration time can also be extended without the use of the VD signal by changing the count field of a Frame Table entry. A line table can be configured as integration time minimum unit and called repeatedly to create the desired integration time.

GENERAL PURPOSE REGISTERS

There are 8 General Purpose Registers. The functionality of these registers are detailed in the KSC-1000 Device Performance Specification. The programming of some of the fields of the General Setup Register, along with the INTG_STRT Setup Register, and the INTG_STRT Line Register are described below.

General Setup Register

The values programmed in the General Setup Register are application dependent. For purposes of the discussion below, the following assumptions are made:

1. There is no over clocking of the horizontal shift register
2. It is desired to store only the active pixels
3. Line rate clamping occurs on the leading dark pixels
4. The CLPDM and CLPOB signals start and stop at the same pixel locations

The value programmed in the Pixels Per Line field is dependent upon the mode of image sensor operation. A value of 4076 is required to for the Single Output Full Image Readout configured with Frame Table 1. A value of 2040 is required for the Fast Dump Decimated Readout mode configured in Frame Table 0, assuming dual output readout is used.

The Line Valid signal is typically used as a sync signal by an external framestore. For the Single Output Full Image Readout mode, the Line Valid Pixel Start field is programmed to a value of 36. This causes the 4 leading dummy pixels, the 20 leading dark pixels, and the 12 active buffer pixels to be discarded by the framestore. The Line Valid Pixel End field is programmed to a value of 4044. This will discard the 12 trailing active buffer pixels and the 20 trailing dark pixels. For the Fast Dump Decimated Readout mode, the Line Valid Pixel Start field is programmed to a value of 36. This causes the 4 dummy pixels, the 20 dark pixels, and the 12 active buffer pixels to be discarded at each output. The Line Valid Pixel End field is programmed to a value of 2040, as there is nothing to discard at the end of a line in dual channel readout mode.

CLPOB_1 and CLPDM_1 are used for frame rate clamping. For the Single Output Full Image Readout mode, a value of 6 is programmed to the CLPDM_1 Pixel Start and CLPOB_1 Pixel Start fields. The CLPOB_1 Pixel End and CLPDM_1 Pixel End fields are programmed to a value of 4074. For the Fast Dump Decimated Readout mode, a value of 6 is programmed to the CLPDM_1 Pixel Start and CLPOB_1 Pixel Start fields. The CLPOB_1 Pixel End and CLPDM_1 Pixel End fields are programmed to a value of 2040. These selections allow clamping on the entire dark row with the exception of 2 pixels on either edge.

CLPOB_2 and CLPDM_2 are used for line rate clamping. For the Single Output Full Image Readout mode, a value of 6 is programmed to the CLPDM_2 Pixel Start and CLPOB_2 Pixel Start fields. The CLPOB_2 Pixel End and CLPDM_2 Pixel End fields are programmed to a value of 22. These selections allow clamping on the leading dark pixels with the exception of the 2 edge pixels. For the Fast Dump Decimated Readout mode, a value of 6 is programmed to the CLPDM_2 Pixel Start and CLPOB_2 Pixel Start fields. The CLPOB_2 Pixel End and CLPDM_2 Pixel End fields are programmed to a value of 22. These selections allow clamping on the leading edge dark pixels with the exception of the 2 boundary pixels on either side.

PBLK is typically used to provide a blanking signal during the vertical clocking interval. For this application, the PBLK Pixel Start field is programmed the value in the Pixels Per Line field. The PBLK Pixel End field is programmed to a value of 0.

There are 14 enable bits for the all of the pixel clock rate outputs. For this example, the following assumptions regarding the pixel rate output clocks are made. 4 horizontal clock signals are required to implement selectable single or dual channel outputs. H1, H2, H3, and H4 are used for the horizontal clocks. SH1, SH2, SH3, SH4, DATACLK1 are used to drive the 2 AFE chips required for dual channel mode. DATACLK2 is used to clock image data into an external image memory.

There are 13 24mA enable bits for all of the pixel rate outputs with the exception of PIXCLK. The 24mA drive selection provides faster rise and fall times. For this example, it is assumed that the 12mA drive is not used for any of the selected outputs.

Finally, there are 4 bits to select the proper DLL for the desired pixel clock frequency. DLL 9 is chosen for the 30MHz pixel clock frequency.

The bit stream for Register 1 configured for dual channel readout is shown in Table 34 below.

Label	Bit Field Width	Data	Bit Stream
Register Address	5	2	01000
Pixels Per Line		2040	0001111111100
Line Valid Pixel Start	13	36	0010010000000
Line Valid Pixel Quadrature Start	2	0	
Line Valid Pixel End	13	2040	0001111111100
CLPOB1_Pix_Start	13	6	0110000000000
CLPOB1_Pix_End	13	2040	0001111111100
CLPOB2_Pix_Start		6	0110000000000
CLPOB2_Pix_End	13	22	0110100000000
CLPDM1_Pix_Start	13	6	
CLPDM1_Pix_End	13	2040	0001111111100
CLPDM2_Pix_Start	13	6	0110000000000
CLPDM2_Pix_End	13	22	0110100000000
PBLK_Pix_Start		2040	0001111111100
PBLK_Pix_End	13	0	0000000000000
Pixel Rate Clock Enable Bits	14		10101111011111
Pixel Rate Clock 24mA Drive Enable Bits	13		0000000000000
DLL Select Bits	4	9	1001

Table 35 General Setup Register Bit Stream for Dual Channel Readout

INTG_STRT Setup Register

The KSC-1000 inserts a shutter pulse after the end the horizontal readout and before the start of the vertical clocking interval. Referring to Timing Requirements in Table 2 on page 6, the KAI-11000 requires a shutter pulse of 5uS and a shutter pulse delay of 1.6uS. With a 25nS pixel clock period, 40 pixel clocks are required to generate a 1uS period. The shutter setup time is the horizontal delay time of 3uS.

Table 36 is a register map of the INTG_STRT Setup Register.

Label	Value	Time	Comment
INTG_STRT Setup Time	106	3.5uS	109 33nS clock period required for 3.5uS Setup Time
INTG_STRT Pulse Width	121	4uS	121 33nS clock periods required for 4uS Pulse Width
INTG_STRT Hold Time	45	1.5uS	45 33nS clock periods required for 1.5uS Hold Time

Table 36 INTG_STRT Setup Register Map

Table 37 illustrates the serial bit stream required to program the INTG_STRT register with the values shown in Table 36. The register fields are programmed from top to bottom as listed in the KSC-1000 Device Performance Specification. Each register field must be programmed with the LSB first. This format holds true for all of the General Purpose Registers.

Register Address Label	RNW	A0	A1	A2	A3
Register Address Bit Stream	0	1	1	0	0
Data Entry Label	**INTG_STRT Setup**	**INTG_STRT Pulse Width**	**INTG_STRT HOLD**		
Bit Stream	0101011000	1001111000	1011010000		

Table 37 INTG_STRT Setup Register Serial I Bit Stream

INTG_STRT Line Register

The value in the INTG_STRT Line register is compared to the vertical line counter. When a match occurs the INTG_STRT signal is inserted prior to the vertical interval. Proper management of counter incrementing and clearing in the line tables is required to produce the expected results.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial release

Table 38 Revision History